IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

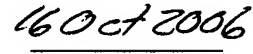|	
Applicant: Morgan	Art Unit: 2674
Serial No.: 09/088,674	Examiner: Nguyen, Kevin M.
Filed: 06/02/1998	Docket No. TI-25995

For: BOUNDARY DISPERSION FOR ARTIFACT MITIGATION

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

15 October 2006

Mails Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

The following Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final Rejection mailed 15 November 2005. Please charge all required fees, including any extension of time fees, to the deposit account of Texas Instruments Incorporated, Deposit Account No. 20-0668.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, to whom this application is assigned.

RELATED APPEALS AND INTERFERENCES

The Appeal Briefs were filed on 3 June 2002, 4 August 2003, and 15 November 2004 in support of the present application. Prosecution was reopened in each case.

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There are no other related appeals or interferences known to the Applicant's legal representative.

STATUS OF THE CLAIMS

This application was filed on 2 June 1998 with ten claims, two of which were written in independent form. An amendment broadening the independent claims, Claim 1 and 6, was filed on 4 October 2000 and has been entered. Claims 1-10 have been rejected and are under appeal herein.

STATUS OF THE AMENDMENTS

A response to the final rejection was submitted 15 May 2006, but did not amend any claims.

SUMMARY OF CLAIMED SUBJECT MATTER

Line 22 of page 2 through line 16 of page 3 of the specification provides a concise explanation of the problem to be solved by the instant invention. Specifically, in real images, boundary conditions often exist where many display picture elements, or pixels, are spatially bunched together with similar image data. If the display system uses pulse width modulation (PWM) and the image data for the pixels has clusters of pixels that cross a major bit transition, PWM artifacts can occur.

The specification, from line 21 of page 3 through line 10 of page 5, provides a concise explanation of the invention defined in appealed independent Claim 1.

The present invention uses boundary dispersion to selectively offset nominal pixel values alternately between a positive offset and a negative offset, repeatedly over a sequence of displayed frames, whereby the average value of the two offset values over the displayed frames, as seen by the viewer, is equal to the nominal pixel value. For

purpose of clarity the frame sequence described below refers to subsequent frames of source video data; however, the sequence can also be comprised of sub-frames within one frame of source video data. The chosen offset may be fixed, or may vary as a function of the nominal pixel value, the pixel spatial location on the screen, and pixel temporal location in time. The set of offsets applied to pixel values typically is varied over a repeating two-frame, or sub-frame, sequence. Selected offsets typically are applied to pixel values within each frame as a function of spatial location on the DMD, and which of the two-frames is being displayed. Within one frame, any given pixel value is offset by some amount above its correct value, and offset the same amount below its normal value in the next frame. Alternatively, the given pixel value is offset below its normal value in the first frame, and then offset above its normal value in the next frame. In either case, the average pixel value over the two-frames, as perceived by the viewer, is the nominal pixel value. The same is true of all pixels displayed on the DMD where an offset is used.

Boundary dispersion offsets certain pixel values from their nominal values in each frame according to preplanned spatial patterns. The spatial pattern used typically is dependent upon the value of the pixel codes. In each spatial pattern, some pixel values get a positive offset and some get a negative offset. In the next frame, an inverse set of offsets are used so that all pixels average to their nominal values over the consecutive two-frame sequence.

A cluster of pixel codes at or near the transition of a major bit (e.g. 8, 16, 32, 64, 128 LSBs) use the offsets so that some pixels have a major bit set, and some without. Adjacent clusters of pixels, where one cluster contains pixels below the major bit and

others contain pixels above the major bit, have the bit transition boundary dispersed. PWM contouring reduction is the result. The offsetting of some pixels positive and some negative in any given frame according to the spatial pattern also prevents any potential flicker artifacts that may be introduced by offsetting pixel codes over two frames.

A checkerboard pattern for a two-frame sequence is one predefined pattern used to a disperse bit transition spatially around a bit transition boundary, for instance, the bit B5, which corresponds to the value of 32. Areas of the screen around this bit transition, for instance, codes 26 through 29, use more complex two-frame patterns. The added complexity of these patterns is needed to control the density of pixels that have a major bit, e.g. B5, set in any given frame. A balance is struck between reducing PWM boundary artifacts and new artifacts introduced within a spatial area having a given code. This is because if to many (or to few) pixels have the major bits set, within an area using a given code, temporal noise can result in this area. The patterns are properly defined so that the contouring artifacts within a code (intra-code) are much less objectionable than the major bit transition boundaries (inter-code boundaries). By use of a particular pattern, for instance the checkerboard pattern, the spatial patterns have pixels with and without the major bits set are packed so spatially tightly that the intra-code contouring is not resolvable by a viewer at normal viewing distance. Since the PWM contouring is dispersed over a larger area, the overall temporal artifacts seen in the image are greatly reduced.

The specification, on lines 4-29 of page 13, and referencing Figure 4, provides a concise explanation of the invention defined in appealed independent Claim 6.

The invention recited by Claim 6 uses a display device such as a binary spatial light modulator comprised of an array of elements each having two states, on and off, one example of which is a digital micromirror device (see lines 8-9 of page 1 and lines 5-21 of page 2 of the original specification).

A degamma function 30 is applied to each RGB color so that the DMD display output matches a CRT response. Since the degamma output is limited to 24 bits, a spatial contouring filter is included that diffuses the 8-bit per color quantization errors for low intensity pixels. The boundary dispersion logic 32 according to the present invention accepts the spatial contouring filter output. The boundary dispersion logic 32 receives signals to identify pixels spatially on the DMD, which signals are provided on signal lines row count ROWCNT and column count COLUMNCNT. A signal is also provided to identify the particular frame of the two-frame temporal sequence, identified as signal FRAME 1/2. A logic high on this line indicates a FRAME 1, and a logic 0 indicates FRAME 2. The boundary dispersion logic assigns spatial patterns as a function of these signals where offsets are applied to each 8-bit color pixel. The offset values are provided to the boundary dispersion logic 32 so that the correct offset is added or subtracted to each pixel in a particular spatial-temporal assignment, as shown in Figure 2 and illustrated in Table 1. The offsets and spatial-temporal patterns applied by the boundary dispersion logic 32 are also a function of the pixel codes. Table 1 illustrates this. Figure 2 illustrates how the boundary dispersion logic is applied to pixels in a spatial-temporal manner.

The 24 signals from the boundary dispersion logic 32 are input into the DMD data formatting logic 40. The DMD data formatting logic organizes the input data into words

which form digital planes of information and then loads them into banks of RAM 42. Data is written to one bank of RAM 40 while the other bank is being continuously read and written to the DMD. Thus, a double-buffer memory is used. The buffers are swapped at each VSYNC which indicates a frame boundary for source pixels.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1.   Whether Claims 1-10 are anticipated under 35 U.S.C. § 102(e) by U.S. Patent No. 6,222,515 to Yamaguchi *et al.*

2.   Whether Claims 4 and 9 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 6,222,515 to Yamaguchi *et al.* in view of U.S. Patent No. 5,731,802 to Aras *et al.*

ARGUMENT

Claim 1:

Claim 1 was rejected under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent No. 6,222,515 to Yamaguchi *et al.* ("Yamaguchi"). The applicant respectfully disagrees and submits the Examiner has failed to establish a prima facie case of anticipation under 35 U.S.C. § 102.

"A person shall be entitled to a patent unless," creates an initial presumption of patentability in favor of the applicant. 35 U.S.C. § 102. "We think the precise language of 35 U.S.C. § 102 that, 'a person shall be entitled to a patent unless,' concerning novelty and unobviousness, clearly places a burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103, see Graham and Adams." *In re Warner*, 379 F.2d 1011, 1016 (C.C.P.A. 1967) (referencing *Graham v. John Deere Co.*, 383 U.S. 1 (1966) and *United States v. Adams*,

383 U.S. 39 (1966)). "As adapted to *ex parte* procedure, *Graham* is interpreted as

continuing to place the 'burden of proof on the Patent Office which requires it to produce

the factual basis for its rejection of an application under sections 102 and 103'." *In re*

Piasecki, 745 F.2d 1468 (Fed. Cir. 1984) (citing *In re Warner*, 379 F.2d at 1016).

"The *prima facie* case is a procedural tool which, as used in patent examination

(as by courts in general), means not only that the evidence of the prior art would

reasonably allow the conclusion the examiner seeks, but also that the prior art compels

such a conclusion if the applicant produces no evidence or argument to rebut it." *In re*

Spada, 911 F.2d 705, 708 n.3 (Fed. Cir. 1990).

The applicant respectfully submits the Examiner has failed to meet the burden of

proof required to establish a prima facie case of anticipation. Section 2131 of the Manual

of Patent Examiner's Procedure provides:

> "'A claim is anticipated only if each and every element as set forth in the
>
> claim is found, either expressly or inherently described in a single prior art
>
> reference.' *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628,
>
> 631, 2 USPQ2d 1051, 1053, (Fed. Cir. 1987). . . . 'The identical invention
>
> must be shown in as complete detail as contained in the . . . claim.'
>
> *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913,
>
> 1920 (Fed. Cir. 1989). The elements must be arranged as in the claim
>
> under review . . . . *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir.
>
> 1990)."

With respect to independent Claim 1, the Examiner has failed to provide a *prima*

facie case of anticipation because the Examiner failed to provide any teaching in

Yamaguchi of "offsetting a first pixel value a first predetermined amount to form a first

offset pixel value and displaying said first offset pixel value during a first display frame;

and offsetting said first pixel value by the opposite of said first predetermined amount to

form a second offset pixel value and displaying said second offset pixel value during a

second display frame, such that the average of said displayed first offset pixel value and

said second offset pixel value is said first pixel value" as recited by Claim 1.

The applicant respectfully submits Yamaguchi does not show, teach, or suggest

"offsetting a first pixel value a first predetermined amount to form a first offset pixel

value" as recited by Claim 1.

To anticipate the claim, Yamaguchi must teach "offsetting a first pixel value,"

which requires Yamaguchi to first have a first pixel value and then offset it. Yamaguchi

fails to teach this.

The Examiner stated, "As to claim 1 (currently revised), Yamaguchi et al teach a

system of displaying digital video data associated with a method comprising: a first pixel

value defined by [(3V) is mean effective voltage], see fig. 7B." A careful reading of

Yamaguchi shows that the 3V signal is not a pixel data value, but rather a desired voltage

signal corresponding to a gray scale intensity level that can be synthesized by selection,

using the pixel data, of a 2V and a 4V signal given the proper timing.

Even is 3V was considered to be a pixel data value, the 3V signal is not offset, in

fact it doesn't appear to even exist in Yamaguchi's embodiment, but rather is the average

of two voltages used to create a gray scale level. Thus, Yamaguchi doesn't offset the 3V

level by -1V to 2V, and then by +1V to 4V. Yamaguchi doesn't offset a first pixel value,

but rather given a pixel data value corresponding to a gray scale level Yamaguchi uses

two sets of drive voltages so that the pixel data value selects drive voltage levels that result in the correct pixel intensity.

Yamaguchi teaches an apparatus that can realize a multiple gray-scale level display of high quality without increasing a circuit scale by avoiding the use of additional generated voltages. (See column 2, lines 27-29 and lines 42-45.)

Column 8, lines 15-35 of Yamaguchi explain the first embodiment of Yamaguchi illustrated by Figures 1 through 15F—including Figure 7B referenced by the Examiner. Yamaguchi teaches, "A gray-scale level 1 shown in FIGS. 7A to 7D, for example, is realized by applying a voltage of 2 (V) to each of the first and second fields to produce a mean effective voltage of 2 (V) for the one frame. This mean effective voltage is shown by hatching in FIGS. 7A to 7D. A gray-scale level 2 is realized by applying 2 (V) to the first field and 4 (V) to the second field to produce a mean effective voltage of 3 (V) for the one frame. To realize an gray-scale level 3, 6 (V) is applied to the first field and 2 (V) to the second field to produce a mean effective voltage of 4 (V) for the one frame. To realize an gray-scale level 4, 6 (V) is applied to the first field and 4 (V) to the second fields to produce a mean effective voltage of 5 (V) for the one frame. In this way, different voltage levels are applied to the first and second fields, respectively, and differences in mean effective voltages occurring in individual frames can realize more gray-scale levels than the gray-scale levels realized by applied data voltages. Namely, an intermediate gray-scale level between two gray-scale levels due to two applied voltages can be realized by the mean effective voltage only."

Thus, Yamaguchi teaches that to generate the correct desired intensity for a pixel data value corresponding to a first gray scale level, 2 volts is used for each of two fields.

To generate the correct desired intensity for a pixel data value corresponding to a second gray scale level, 2 volts is used during a first field, and 4 volts is used during a second field. Yamaguchi does this precisely because he doesn't have a 3 volt signal and doesn't want to provide a voltage source for each gray scale level. So there is not teaching of offsetting a pixel value, or offsetting a voltage, but rather just using two different voltages, to create some of the pixel values that correspond to the voltage levels that are not provided. To generate the correct desired intensity for a pixel data value corresponding to a third gray scale level, 6 volts is used during a first field, and 2 volts is used during a second field. To generate the correct desired intensity for a pixel data value corresponding to a fourth gray scale level, 6 volts is used during a first field, and 4 volts is used during a second field. In this manner, Yamaguchi uses a data driver that is only able to simultaneously provide two voltage levels (and therefore only create two gray scale levels) in a manner that creates four gray scale levels by changing the voltages provided during two periods. (See column 8, lines 7-10.) During a first period 2 and 6 volts are provided, and during a second period 2 and 4 volts are provided.

Yamaguchi does not have a 3V signal, and therefore cannot offset the 3V signal to provide a 2V and 4V signals. To the contrary, Yamaguchi teaches away from using a 3V signal, by teaching a method of creating additional gray scale levels without using a corresponding number of voltage levels.

The Examiner further states that Yamaguchi et al further teach inherently a first predetermined amount "-1" [defined by an area hatching from 3V to 2V at the first field] to form a first offset pixel value [defined by 2V at the first field], and a displaying said first offset pixel during a first frame period [2V at the first filed, see fig. 7B]."

The applicant respectfully submits that the Examiner is simply stating that what clearly is not taught by Yamaguchi, but is in Claim 1, is inherent in the teachings of Yamaguchi. The Examiner states the first pixel value, for the purposes of his analysis of Claim 1, is 3V. As stated above, Yamaguchi does not actually have a 3V signal and therefore cannot offset the 3V signal by an inherent +/- 1V. Instead, Yamaguchi uses two sets of drive voltages (2V, 6V) and (2V, 4V), to allow a pixel data value to select voltages that average to the desired level.

The Examiner has failed to point to any teaching in Yamaguchi that anticipates the limitations of Claim 1, namely "offsetting a first pixel value a first predetermined amount to form a first offset pixel value" and "offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value."

Yamaguchi's teachings therefore do not set forth each and every element of Claim 1 as required by *Verdegaal*, or show the identical invention in as complete detail as contained in Claim 1 as required by *Richardson*, or arrange the elements as in Claim 1 as required by *In re Bond*. The Examiner's rejection of Claim 1 as anticipated by Yamaguchi therefore is unsupported by Yamaguchi and should be withdrawn.

Claim 2:

Claim 2 was rejected under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent No. 6,222,515 to Yamaguchi *et al*. ("Yamaguchi"). The applicant respectfully disagrees and submits the Examiner has failed to establish a *prima facie* case of anticipation under 35 U.S.C. § 102.

Claim 2 depends from Claim 1 and should be deemed allowable for that reason and on its own merits. For the reasons given above with respect to Claim 1, the Examiner has failed to present a *prima facie* case of anticipation with respect to Claim 1.

Claim 2 recites, "the value of said first predetermined amount is selected as a function of said first pixel value." The Examiner stated, "Yamaguchi et al teach inherently said first predetermined amount "-1" [defined by 2V-3V at the first field], said predetermined amount "+1" [defined by 4V-3V at the first field]. Thus, said first predetermined amount "-1" is selectively as a function of (X-3)."

The applicant respectfully submits this analysis is not clear and does not show anticipation of Claim 2 by Yamaguchi. As stated above, the 3V referred to by the Examiner is not the pixel data value, but rather the LCD drive voltage needed to select the proper intensity level. Yamaguchi, rather than provide a complex circuit capable of providing the proper drive voltage for every desired gray-scale level, teaches a method of alternately using drive voltages to create more gray scale levels than would be available without alternately using the drive voltages. Yamaguchi does not offset the pixel data value, nor does Yamaguchi teach "a function of (X-3)" as suggested by the Examiner.

The Examiner has failed to point to any teaching in Yamaguchi that anticipates the limitations of Claim 2, namely "the value of said first predetermined amount is selected as a function of said first pixel value."

Yamaguchi's teachings therefore do not set forth each and every element of Claim 2 as required by *Verdegaal*, or show the identical invention in as complete detail as contained in Claim 2 as required by *Richardson*, or arrange the elements as in Claim 2 as

required by *In re Bond*. The Examiner's rejection of Claim 2 as anticipated by Yamaguchi therefore is unsupported by Yamaguchi and should be withdrawn.

Claim 3:

Claim 3 was rejected under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent No. 6,222,515 to Yamaguchi *et al.* ("Yamaguchi"). The applicant respectfully disagrees and submits the Examiner has failed to establish a *prima facie* case of anticipation under 35 U.S.C. § 102.

Claim 3 depends from Claim 1 and should be deemed allowable for that reason and on its own merits. For the reasons given above with respect to Claim 1, the Examiner has failed to present a *prima facie* case of anticipation with respect to Claim 1.

Claim 3 recites, "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed." Lines 28-30 of page 3, and line 24 of page 4 through line 10 of page 5, as well as other passages of the original specification, provide support for this claim limitation.

The Examiner stated, "Yamaguchi et al teach said first offset pixel value 2V is less than said first pixel value (3V) as a function (X-3) of the spatial location ["-1" defined the spatial location] that [(3V) is mean effective voltage] defined to be displayed."

The applicant respectfully submits this analysis is not clear and does not show anticipation of Claim 3 by Yamaguchi. The Examiner does not appear to make any coherent argument that Yamaguchi shows, teaches, or suggests a "function of the spatial location" as required by Claim 3.

The Examiner has failed to point to any teaching in Yamaguchi that anticipates the limitations of Claim 3, namely "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed."

Yamaguchi's teachings therefore do not set forth each and every element of Claim 3 as required by *Verdegaal*, or show the identical invention in as complete detail as contained in Claim 3 as required by *Richardson*, or arrange the elements as in Claim 3 as required by *In re Bond*. The Examiner's rejection of Claim 3 as anticipated by Yamaguchi therefore is unsupported by Yamaguchi and should be withdrawn.

Claim 4:

Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,222,515 to Yamaguchi *et al.* ("Yamaguchi") in view of U.S. Patent No. 5,731,802 to Aras *et al.* ("Aras"). The applicant respectfully disagrees and submits the Examiner has failed to establish a *prima facie* case of obviousness under 35 U.S.C. § 103.

"To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). 'All words in a claim must be considered in judging the patentability of that claim against the prior art.' *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.

"To support the conclusion that the claimed combination is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed combination or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the

teachings of the references." *Ex parte Clapp*, 227 U.S.P.Q. 972, 973 (Bd. Pat. App. & Inter. 1985).

The Examiner has failed to meet the duty of presenting a prima facie obviousness rejection. Claim 4 depends from Claim 1 and should be deemed allowable for that reason and on its own merits. For the reasons given above with respect to Claim 1, the Examiner has failed to present a *prima facie* case of anticipation with respect to Claim 1.

Claim 4 further recites, "said pixel values are displayed using a plurality of weighted bit-planes" and "said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame." Lines 16-23 of page 4, as well as other passages of the original specification, provide support for this claim limitation.

The Examiner stated, "Yamaguchi et al teach all of the claimed limitations of claims 1 and 6, except for display uses a plurality of weighted bit-plane, wherein said first pixel values close to a bit transition of said bit-planes are offset during said display frame and said second frame. However, Aras et al teach the number of rows multiplied by the number of bits in grayscale weighting is equal to the number of update even per frame or write cycle per frame (fig. 4, col. 5, lines 32-34). Rows 0, 1 and 2 are loaded with the data for the 0th, 3rd and 2nd weight bits, respectively. The number of data transitions per clock cycle during the next clock cycle of the data in rows 1 and 2 changes such that rows 1 and 2 are loaded with the data for its 0th and 3rd weight bits, respectively (col. 5, lines 26-37). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Yamaguchi et al's field (frame, fig. 7) including rows 0, 1 and 2 are loaded with the data for the 0th, 3rd, and 2nd weight bits,

respectively. The number of data transitions per clock cycle during the next clock cycle of the data in rows 1 and 2 changes such that rows 1 and 2 are loaded with the data for its 0th and 3rd weight bits, respectively, in view of the teaching in the Aras et al's reference, because this would provide gray scale using a weighted PWM scheme which does not flicker and provides a reduced bandwidth requirement for the associated control circuitry and data bus as taught by Aras et al (col. 3, lines 41-44)."

The applicant respectfully submits this analysis is far from clear and does not present a *prima facie* case of obviousness of Claim 4 by Yamaguchi in view of Aras. The Examiner does not appear to make any coherent argument that Yamaguchi, in view of Aras shows, teaches, or suggests a "said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame" as required by Claim 4, nor does the Examiner point to any teaching in the prior art references that expressly or impliedly suggests the claimed combination, or present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references as required by *Ex parte Clapp*. The Examiner's rejection of Claim 4 as unpatentable over Yamaguchi in view of Aras therefore is unsupported by the prior art and should be withdrawn.

Claim 6:

Claim 6 was rejected under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent No. 6,222,515 to Yamaguchi *et al.* ("Yamaguchi"). The applicant respectfully disagrees and submits the Examiner has failed to establish a prima facie case of anticipation under 35 U.S.C. § 102.

With respect to independent Claim 6, the Examiner has failed to provide a *prima facie* case of anticipation because the Examiner failed to provide any teaching in Yamaguchi of "a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value" as recited by Claim 6.

The applicant respectfully submits Yamaguchi does not show, teach, or suggest "a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value" as recited by Claim 6.

To anticipate the claim, Yamaguchi must teach "a logic circuit offsetting a first pixel value," which requires Yamaguchi to first have a first pixel value and then offset it using a logic circuit. Yamaguchi fails to teach this.

The Examiner stated, "As to claim 6 (currently revised), Yamaguchi et al teach inherently a logic circuit defined by means for offsetting inherently a first predetermined amount "-1" [defined by an area hatching from 3V to 2V at the first field] to form a first offset pixel value [defined by 2V at the first field] Yamaguchi et al further teach inherently a logic circuit defined by means for offsetting inherently by the opposite of said predetermined amount "+1" [defined by an area hatching from 3V to 4V at the said second field] to form a second offset pixel value [defined by 4V at a second field]."

As discussed above with respect to Claim 1, a careful reading of Yamaguchi shows that the 3V signal is not a pixel data value, but rather a desired voltage signal corresponding to a gray scale intensity level that can be synthesized by selection, using the pixel data, of a 2V and a 4V signal given the proper timing.

Even is 3V was considered to be a pixel data value, the 3V signal is not offset, in fact it doesn't appear to even exist in Yamaguchi's embodiment, but rather is the average of two voltages used to create a gray scale level. Thus, Yamaguchi doesn't offset the 3V level by -1V to 2V, and then by +1V to 4V. Yamaguchi doesn't offset a first pixel value, but rather given a pixel data value corresponding to a gray scale level Yamaguchi uses two sets of drive voltages so that the pixel data value selects drive voltage levels that result in the correct pixel intensity.

Yamaguchi teaches an apparatus that can realize a multiple gray-scale level display of high quality without increasing a circuit scale by avoiding the use of additional generated voltages. (See column 2, lines 27-29 and lines 42-45.)

Column 8, lines 15-35 of Yamaguchi explain the first embodiment of Yamaguchi illustrated by Figures 1 through 15F—including Figure 7B referenced by the Examiner. Yamaguchi teaches, "A gray-scale level 1 shown in FIGS. 7A to 7D, for example, is realized by applying a voltage of 2 (V) to each of the first and second fields to produce a mean effective voltage of 2 (V) for the one frame. This mean effective voltage is shown by hatching in FIGS. 7A to 7D. A gray-scale level 2 is realized by applying 2 (V) to the first field and 4 (V) to the second field to produce a mean effective voltage of 3 (V) for the one frame. To realize an gray-scale level 3, 6 (V) is applied to the first field and 2 (V) to the second field to produce a mean effective voltage of 4 (V) for the one frame. To realize an gray-scale level 4, 6 (V) is applied to the first field and 4 (V) to the second fields to produce a mean effective voltage of 5 (V) for the one frame. In this way, different voltage levels are applied to the first and second fields, respectively, and differences in mean effective voltages occurring in individual frames can realize more

gray-scale levels than the gray-scale levels realized by applied data voltages. Namely, an intermediate gray-scale level between two gray-scale levels due to two applied voltages can be realized by the mean effective voltage only."

Thus, Yamaguchi teaches that to generate the correct desired intensity for a pixel data value corresponding to a first gray scale level, 2 volts is used for each of two fields. To generate the correct desired intensity for a pixel data value corresponding to a second gray scale level, 2 volts is used during a first field, and 4 volts is used during a second field. Yamaguchi does this precisely because he doesn't have a 3 volt signal and doesn't want to provide a voltage source for each gray scale level. So there is not teaching of offsetting a pixel value, or offsetting a voltage, but rather just using two different voltages, to create some of the pixel values that correspond to the voltage levels that are not provided. To generate the correct desired intensity for a pixel data value corresponding to a third gray scale level, 6 volts is used during a first field, and 2 volts is used during a second field. To generate the correct desired intensity for a pixel data value corresponding to a fourth gray scale level, 6 volts is used during a first field, and 4 volts is used during a second field. In this manner, Yamaguchi uses a data driver that is only able to simultaneously provide two voltage levels (and therefore only create two gray scale levels) in a manner that creates four gray scale levels by changing the voltages provided during two periods. (See column 8, lines 7-10.) During a first period 2 and 6 volts are provided, and during a second period 2 and 4 volts are provided.

Yamaguchi does not have a 3V signal, and therefore cannot offset the 3V signal to provide a 2V and 4V signals. To the contrary, Yamaguchi teaches away from using a

3V signal, by teaching a method of creating additional gray scale levels without using a corresponding number of voltage levels.

The Examiner further states that Yamaguchi et al further teach inherently a first predetermined amount "-1" [defined by an area hatching from 3V to 2V at the first field] to form a first offset pixel value [defined by 2V at the first field], and a displaying said first offset pixel during a first frame period [2V at the first filed, see fig. 7B]."

The applicant respectfully submits that the Examiner is simply stating that what clearly is not taught by Yamaguchi, but is in Claim 6, is inherent in the teachings of Yamaguchi. The Examiner states the first pixel value, for the purposes of his analysis of Claim 6, is 3V. As stated above, Yamaguchi does not actually have a 3V signal and therefore cannot offset the 3V signal by an inherent +/- 1V much less using an inherent logic circuit. Instead, Yamaguchi uses two sets of drive voltages (2V, 6V) and (2V, 4V), to allow a pixel data value to select voltages that average to the desired level.

The Examiner has failed to point to any teaching in Yamaguchi that anticipates the limitations of Claim 6, namely "offsetting a first pixel value a first predetermined amount to form a first offset pixel value" and "offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value."

Yamaguchi's teachings therefore do not set forth each and every element of Claim 6 as required by *Verdegaal*, or show the identical invention in as complete detail as contained in Claim 6 as required by *Richardson*, or arrange the elements as in Claim 6 as required by *In re Bond*. The Examiner's rejection of Claim 6 as anticipated by Yamaguchi therefore is unsupported by Yamaguchi and should be withdrawn.

Claim 7:

Claim 7 was rejected under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent No. 6,222,515 to Yamaguchi *et al.* ("Yamaguchi"). The applicant respectfully disagrees and submits the Examiner has failed to establish a *prima facie* case of anticipation under 35 U.S.C. § 102.

Claim 7 depends from Claim 6 and should be deemed allowable for that reason and on its own merits. For the reasons given above with respect to Claim 6, the Examiner has failed to present a *prima facie* case of anticipation with respect to Claim 6.

Claim 7 recites, "the value of said first predetermined amount is selected by said logic circuit as a function of said first pixel value." The Examiner stated, "Yamaguchi et al teach inherently said first predetermined amount "-1" [defined by 2V-3V at the first field], said predetermined amount "+1" [defined by 4V-3V at the first field]. Thus, said first predetermined amount "-1" is selectively as a function of (X-3)."

The applicant respectfully submits this analysis is not clear and does not show anticipation of Claim 7 by Yamaguchi. As stated above, the 3V referred to by the Examiner is not the pixel data value, but rather the LCD drive voltage needed to select the proper intensity level. Yamaguchi, rather than provide a complex circuit capable of providing the proper drive voltage for every desired gray-scale level, teaches a method of alternately using drive voltages to create more gray scale levels than would be available without alternately using the drive voltages. Yamaguchi does not offset the pixel data value, nor does Yamaguchi teach "a function of (X-3)" as suggested by the Examiner.

The Examiner has failed to point to any teaching in Yamaguchi that anticipates the limitations of Claim 7, namely "the value of said first predetermined amount is selected by said logic circuit as a function of said first pixel value."

Yamaguchi's teachings therefore do not set forth each and every element of Claim 7 as required by *Verdegaal*, or show the identical invention in as complete detail as contained in Claim 7 as required by *Richardson*, or arrange the elements as in Claim 7 as required by *In re Bond*. The Examiner's rejection of Claim 7 as anticipated by Yamaguchi therefore is unsupported by Yamaguchi and should be withdrawn.

Claim 8:

Claim 8 was rejected under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent No. 6,222,515 to Yamaguchi *et al*. ("Yamaguchi"). The applicant respectfully disagrees and submits the Examiner has failed to establish a *prima facie* case of anticipation under 35 U.S.C. § 102.

Claim 8 depends from Claim 6 and should be deemed allowable for that reason and on its own merits. For the reasons given above with respect to Claim 6, the Examiner has failed to present a *prima facie* case of anticipation with respect to Claim 6.

Claim 8 recites, "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed." Lines 28-30 of page 3, and line 24 of page 4 through line 10 of page 5, as well as other passages of the original specification, provide support for this claim limitation.

The Examiner stated, "Yamaguchi et al teach said first offset pixel value 2V is less than said first pixel value (3V) as a function (X-3) of the spatial location ["-1" defined the spatial location] that [(3V) is mean effective voltage] defined to be displayed."

The applicant respectfully submits this analysis is not clear and does not show anticipation of Claim 8 by Yamaguchi. The Examiner does not appear to make any coherent argument that Yamaguchi shows, teaches, or suggests a "function of the spatial location" as required by Claim 8.

The Examiner has failed to point to any teaching in Yamaguchi that anticipates the limitations of Claim 8, namely "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed."

Yamaguchi's teachings therefore do not set forth each and every element of Claim 8 as required by *Verdegaal*, or show the identical invention in as complete detail as contained in Claim 8 as required by *Richardson*, or arrange the elements as in Claim 8 as required by *In re Bond*. The Examiner's rejection of Claim 8 as anticipated by Yamaguchi therefore is unsupported by Yamaguchi and should be withdrawn.

Claim 9:

Claim 9 was rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,222,515 to Yamaguchi *et al.* ("Yamaguchi") in view of U.S. Patent No. 5,731,802 to Aras *et al.* ("Aras"). The applicant respectfully disagrees and submits the Examiner has failed to establish a *prima facie* case of obviousness under 35 U.S.C. § 103.

The Examiner has failed to meet the duty of presenting a prima facie obviousness rejection. Claim 9 depends from Claim 6 and should be deemed allowable for that reason and on its own merits. For the reasons given above with respect to Claim 6, the Examiner has failed to present a *prima facie* case of anticipation with respect to Claim 6.

Claim 9 further recites, "said pixel values are displayed using a plurality of weighted bit-planes" and "said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame." Lines 16-23 of page 4, as well as other passages of the original specification, provide support for this claim limitation.

The Examiner stated, "Yamaguchi et al teach all of the claimed limitations of claims 1 and 6, except for display uses a plurality of weighted bit-plane, wherein said first pixel values close to a bit transition of said bit-planes are offset during said display frame and said second frame. However, Aras et al teach the number of rows multiplied by the number of bits in grayscale weighting is equal to the number of update even per frame or write cycle per frame (fig. 4, col. 5, lines 32-34). Rows 0, 1 and 2 are loaded with the data for the 0th, 3rd and 2nd weight bits, respectively. The number of data transitions per clock cycle during the next clock cycle of the data in rows 1 and 2 changes such that rows 1 and 2 are loaded with the data for its 0th and 3rd weight bits, respectively (col. 5, lines 26-37). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Yamaguchi et al's field (frame, fig. 7) including rows 0, 1 and 2 are loaded with the data for the 0th, 3rd, and 2nd weight bits, respectively. The number of data transitions per clock cycle during the next clock cycle of the data in rows 1 and 2 changes such that rows 1 and 2 are loaded with the data for its 0th and 3rd weight bits, respectively, in view of the teaching in the Aras et al's reference, because this would provide gray scale using a weighted PWM scheme which does not flicker and provides a reduced bandwidth requirement for the associated control circuitry and data bus as taught by Aras et al (col. 3, lines 41-44)."

The applicant respectfully submits this analysis is far from clear and does not present a *prima facie* case of obviousness of Claim 9 by Yamaguchi in view of Aras. The Examiner does not appear to make any coherent argument that Yamaguchi, in view of Aras shows, teaches, or suggests a "said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame" as required by Claim 9, nor does the Examiner point to any teaching in the prior art references that expressly or impliedly suggests the claimed combination, or present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references as required by *Ex parte Clapp*. The Examiner's rejection of Claim 9 as unpatentable over Yamaguchi in view of Aras therefore is unsupported by the prior art and should be withdrawn.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-10 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

Please charge any fees necessary in connection with the filing of this paper, including any necessary extension of time fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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CLAIMS APPENDIX

1. (Previously presented) A method of displaying digital video data comprising pixel values, said method comprising the steps of:

   offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and

   offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

2. (Original) The method as specified in Claim 1 wherein the value of said first predetermined amount is selected as a function of said first pixel value.

3. (Original) The method as specified in Claim 1 wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed.

4. (Original) The method as specified in Claim 1 wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame.

5. (Original) The method as specified in Claim 1 wherein said first display frame and said second display frame are consecutive.

6. (Previously presented) A system of displaying digital video data comprising pixel

values, comprising:

a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and

display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

7.   (Original) The system as specified in Claim 6 wherein the value of said first predetermined amount is selected by said logic circuit as a function of said first pixel value.

8.   (Original) The system as specified in Claim 6 wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed.

9.   (Original) The system as specified in Claim 6 wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame.

10.   (Original) The system as specified in Claim 6 wherein said first display frame and said second display frame are consecutive.

<u>EVIDENCE APPENDIX</u>

None.

RELATED PROCEEDINGS APPENDIX

None.